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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,376	02/20/2004	Georg Braun	INFN/0062	6404

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EXAMINER	
MCFADDEN, MICHAEL B	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,376	BRAUN ET AL.	
	Examiner	Art Unit	
	Michael B. McFadden	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/783,376 has a total of 22 claims pending in the application, there are 3 independent claims and 19 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

3. As required by M.P.E.P. ' 201.14(c), acknowledgment is made of applicant's claim for priority based on an application filed on 21 February 2003.

III. INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted 1 July 2004 are acceptable for examination purposes.

IV. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

5. As required by M.P.E.P. ' 609 (C), the applicant's submission of the Information Disclosure Statement dated 20 February 2004 is acknowledged by the examiner and

the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. ' 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

VII. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-8 and 12-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Haupt (US Patent No. 6,334,159).

8. **Regarding Claims 1, 16, and 22,** Haupt discloses a synchronous memory system **(Haupt: Column 7, Lines 2-4)**, comprising: one or more memory modules in a main memory, with each memory module comprising one or more memory banks **(Haupt: Figure 2, Elements 535A, 535B, 535C, and 535D)**, a memory control device configured to generate commands comprising a plurality of command segments with a respective plurality of elements **(Haupt: Figure 1, Element 120A)**, wherein one of the

command segments is a selection command segment for selecting one or more memory banks, and wherein each of the memory banks has at least one uniquely associated element of the selection command segment, and a transfer bus **(Haupt: Figure 1, Element 130 which includes Figure 2, Elements 510 and 520)** for communication between the memory control device and the memory modules, wherein the transfer bus is in the form of a concatenated bus structure and comprises a plurality of parallel transfer lines; and wherein the memory control device is configured to transfer the commands to the memory modules using the transfer bus, and wherein the transfer bus is configured to transfer the elements of a command segment in parallel. **(Haupt: Column 5, Lines 40-51) It is noted that the POD has the capability to address one of the storage sub-units and therefore inherently possesses a selection command. (Haupt: Column 6, Lines 10-14.)**

9. **Regarding Claims 2 and 17,** Haupt discloses where the memory modules further comprise a buffer device for forwarding the commands to one or more memory banks in at least one of a respective memory module and one or more other memory modules. **(Haupt: Figure 2, Elements 550 and 530)**

10. **Regarding Claims 3 and 18,** Haupt discloses where the buffer device is configured to compare the bit pattern of a given selection command segment with one or more predetermined bit patterns and to determine whether the associated command needs to be forwarded to at least one of: (i) one or more of the memory banks in the memory module, (ii) and one or more other memory modules. **(Haupt: Column 6, Lines 10-14 and Lines 47-52)**

11. **Regarding Claims 4 and 19,** Haupt discloses wherein the buffer device is configured to generate a chip select signal for one or more memory banks. **(Haupt: Column 6, Lines 10-14 and Lines 44-52)**

12. **Regarding Claims 5 and 20,** Haupt discloses where the selection command segment is the first segment of the commands. **The Office notes that the location of the select command is a design choice. Haupt Column 6, Lines 44-55 teaches that it queues memory requests and provides the appropriate requested address.**

13. **Regarding Claim 6,** Haupt discloses wherein the number of transfer lines in the transfer bus is at least equal to the maximum number of memory banks which can be used in the memory system. **(Haupt: Figures 1 and 2)**

14. **Regarding Claims 7 and 8,** Haupt discloses wherein the commands contain an element for a clock enable signal for all the memory banks. **(Haupt: Column 6, Lines 59-63, Column 10, Lines 17-19, and Column 11, Lines 44-56)**

15. **Regarding Claims 12 and 13,** Haupt discloses wherein the commands contain an element for a reset signal and comprising a transfer line connecting the memory control device and at least one of the memory modules and configured to propagate a reset signal. **(Haupt: Column 6, Lines 55-59) The Flush command functions the same as a reset command.**

16. **Regarding Claim 14,** Haupt discloses wherein the commands contain an element for signaling that the command is intended for the buffer device. **(Haupt: Column 6, Lines 47-52 and Lines 59-63) The control commands are intended for**

the buffer and indicate control information the buffer is to apply. Therefore the element to signal that the command is intended for the buffer must be inherent.

17. **Regarding Claims 15 and 21,** Haupt discloses wherein the memory control device comprises a coding device for coding generated commands and the buffer device comprises a decoding device for decoding received coded commands.**(Haupt: Figure 9, Element 1290) The inclusion of a decoding device points to the fact that commands must be decoded. Therefore the inclusion of an encoding device is inherent.**

Claim Rejections - 35 USC ' 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haupt (US Patent No 6,334,159).

20. **Regarding Claims 9, 10, and 11,** Haupt fails to disclose the inclusion of an on-die termination signal.

The Office takes Official Notice that it would have been obvious to a person of ordinary skill in the art to include an on-die termination signal in the memory system of Haupt.

The motivation for doing so would have been to eliminate bouncing and ringing that occurs whenever a signal hits an interface in its path.

Therefore it would have been obvious to include an on-die termination signal in the memory system of Haupt in order to eliminate bouncing and ringing that occurs whenever a signal hits an interface in its path to obtain the invention as described in Claims 9, 10, and 11.

VIII. RELEVANT ART CITED BY THE EXAMINER

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Baji (US Patent No. 5,740,404) discloses a digital signal processor with an on chip select signal and a decoder.

Doasaka et al. (US Patent No. 6,347,063) discloses a multiple module synchronous memory system with parallel data transfer.

IX. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

22. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(4). CLAIMS REJECTED IN THE APPLICATION

23. Per the instant office action, claims 1-22 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. McFadden whose telephone number is (571)272-8013. The examiner can normally be reached on Monday-Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan
5/1/06

MBM
4/28/2006

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER